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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Paper No. 11

Application Number: 09/465,634
Filing Date: December 17, 1999
Appellant(s): VAVRO ET AL.

MAILED

FEB 1 0 2003

Technology Center 2100

Timothy N. Trop
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 15, 2003.

(1)   *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2)   *Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or

be directly affected by or have a bearing on the decision in the pending appeal is contained in the

brief.

(3)   *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4)   *Status of Amendments After Final*

No amendment after final has been filed.

(5)   *Summary of Invention*

The summary of invention contained in the brief is correct.

(6)   *Issues*

The appellant's statement of the issues in the brief is correct.

(7)   *Grouping of Claims*

Examiner acknowledges that Applicant has grouped claims 1-15 separately from claims

16-24, whereby claims 1-15 rise and fall with claim 1 and claims 16-24 rise and fall with claim

16. However, the Board is advised that the Applicant has failed to include reasons to support the

grouping. Applicant has not explained how the two groups of claims differ in scope and are

patentably distinct from each other. See 37 CFR 1.192(c)(7). The only difference that

Examiner notes is that claims 1-15 are device claims and claims 16-24 are method claims.

Furthermore, it is noted that the element of dispute is the term "mathematical", which refers to a

claimed processor, appears in both the method and device claim groups, in claim 1 and claim 16.

Since the element of dispute appears in both groups of claims, Examiner Suggests that the Board

group claims 1-24 together, whereby claims 1-24 rise and fall with claim 1.

(8)   Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9)   Prior Art of Record

EP 0 942 603   Kitamura et al.   9-1999

(10)   Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112

Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for

failing to particularly point out and distinctly claim the subject matter which Applicant regards as

the invention. The claim recites the limitation "wherein said mathematical processor is a multi-

cycled mathematical processor." This language is unclear because since the word "cycle" is a

measurement of time, it is unclear how a processor can be multi-timed. This phraseology in the

claims may have the following two accepted meanings: 1) the processor requires multiple cycles

to complete an operation, or 2) the processor is operated at various cycle speeds. In order to

clear up this interpretation discrepancy, Examiner tried to identify which portion of the

specification in which Applicant refers in order to interpret the term "multi-cycled". However,

there is support for both interpretations in the specification. On page 24, lines 20-23, Applicant

discloses a multi-cycle operation on a processor which may take more than one cycle to

complete, which supports the first meaning of the phraseology. On page 23, line 19, Applicant

discloses a multi-cycle mathematical processor that is operated at various speeds, which supports

the second meaning. After reading claim 15 in light of the specification, claim 15 is still

indefinite. For the purposes of examination, the first meaning is assumed.

Claim Rejections - 35 USC § 102

Claims 1-4, 6, 8, 9, 15, 16, 17, 23, and 24 are rejected under 35 U.S.C. 102(a) as being

anticipated by Kitamura, EP 0942603A2 as labeled document I in Applicant's IDS (hereinafter

Kitamura). Referring to claim 1, Kitamura has taught a digital signal processor comprising:

   a. a mathematical processor (Kitamura column 9, line 58 to column 10, line 1 and figure

   6, element 5, column 26, lines 39-50);

   b. an input processor that processes input signals to the digital signal processor

   (Kitamura column 10, line 28 to column 11, line 8 and figure 6, element 3);

   c. an output processor that processes output signals from the digital signal processor

   (Kitamura column 12, lines 15-52 and figure 6, element 6);

   d. a master processor that controls said mathematical processor, said input processor and

   said output processor (Kitamura column 10, lines 1-2 and figure 6, element 7); and

   e. a storage selectively accessible by each of said processors (Kitamura column 10, lines

   21-27 and figure 6, element 10).

Referring to claim 2, Kitamura has taught the digital signal processor further including a

random access memory processor that stores intermediate calculation results (Kitamura column

12, lines 10-14).

Referring to claim 3, Kitamura has taught the digital signal processor including a bus coupling each of said processors to said storage (Kitamura figure 6, element 9). Referring to claim 4, Kitamura has taught the digital signal processor wherein said input and output processors also implement mathematical operations (Kitamura column 10, line 28 to column 11, line 8, column 12, lines 15-52 and figure 6, elements 3 and 6).

Referring to claim 6, Kitamura has taught the digital signal processor wherein said processors communicate with one another through said storage (Kitamura column 10, lines 15-17 and 28-32, column 11, lines 47-55, and column 12, lines 15-20).

Referring to claim 8, Kitamura has taught the digital signal processor wherein said master processor provides the timing for the other processors (Kitamura column 10, lines 5-14 where the master processor determines the timing for when the processors execute instructions because it controls when the instructions are sent).

Referring to claim 9, Kitamura has taught the digital signal processor wherein said master processor waits for the input processor to complete a given operation (Kitamura column 6, lines 3-20 and column 11, lines 47-49 where the signal must be processed in the input processor before being spliced by the data processing unit as per the control of the master processor, therefore, the master processor must wait for the input processor to complete its operation). Referring to claim 15, Kitamura has taught the digital signal processor wherein said mathematical processor is a multi-cycled mathematical processor (Kitamura column 11, lines 46-55 where an operation takes multiple cycles to complete).

Claim 16 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

Claim 17 does not recite limitations above the claimed invention set forth in claim 3 and is therefore rejected for the same reasons set forth in the rejection of claim 3 above.

Claims 23 and 24 do not recite limitations above the claimed invention set forth in claim 15 and are therefore rejected for the same reasons set forth in the rejection of claim 15 above.

Claim Rejections - 35 USC § 103

Claims 5, 7, 14, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura, EP 0942603A2 as labeled document I in Applicant's IDS (hereinafter Kitamura). Referring to claim 5, Kitamura has not explicitly taught each of said processors having their own instruction sets. However, Kitamura has taught a mathematical processor, an input processor, an output processor, and a master processor each with divergent functionality. Since the definition of an instruction set is that combination of commands which allows a processor to appropriately perform its defined functions, it would be readily acknowledged by an artisan that the plural processors as taught by Kitamura must each have their own instruction set. That is, the instructions required to perform the input processing, mathematical functions, control, and output processing must be different from one another. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to recreate the plural processors of Kitamura where each has its own instruction set. Official notice has been taken.

Referring to claim 7, Kitamura has not explicitly taught each processor using very long instruction words. Employing this type of instruction format is well known in the art and would have allowed for the processors of Kitamura to be issued several instructions at once and ensured, by the nature of VLIW instructions, that the compiler would have only combined instructions that are not dependent upon one another. Therefore, it would have been obvious to a

person of ordinary skill in the art at the time the invention was made to employ the very long

instruction word format for instructions issued to the plural processors of Kitamura in order to

increase speed and efficiency of those processors. Official notice has been taken.

Referring to claim 14, Kitamura has not explicitly taught a mathematical pipeline which

is pipelined. However, Kitamura has taught a mathematical processor that requires multiple

cycles to complete a given operation, i.e. at least one cycle for memory access and one cycle for

execution (Kitamura column 11, lines 51-55). The concept of pipelining is well known in the art

and would have been beneficially employed in the mathematical processor of Kitamura in order

to increase efficiency by overlapping the steps of memory access and execution for each

processed instruction. Therefore, it would have been obvious to a person of ordinary skill in the

art at the time the invention was made to employ the well known concept of pipelining to the

mathematical processor in order to increase efficiency and speedup. Official notice has been

taken.

Claim 22 does not recite limitations above the claimed invention set forth in claim 14 and

is therefore rejected for the same reasons set forth in the rejection of claim 14 above.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura, EP

0942603A2 as labeled document I in Applicant's IDS (hereinafter Kitamura) in view of

Whittaker et al., U.S. Patent Number 5,968,167 (hereinafter Whittaker). Kitamura has not

explicitly taught the digital signal processor wherein each of said processors includes its own

random access memory. Whittaker has taught each of a plurality of processors including its own

random access memory (Whittaker column 6, lines 56-65). The RAMs of Whittaker provide

storage for those instructions to be executed by each processor. As discussed above in the

rejection of claim 5, each processor of Kitamura has its own instruction set and those instructions are issued to each processor by the master processor. Therefore, it would have been beneficial to employ separate RAMs for each processor such that the master processor would have required less logic to inform each processor to access its RAM and fetch its own next instruction, rather than the master accessing the main storage, determining which processor the instruction belonged to, and then physically issuing that instruction to the slave processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ individual RAMs for each of the plural processors of Kitamura, as taught by Whittaker in order to allow for a simpler master processor.

Claims 11-13, and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura, EP 0942603A2 as labeled document I in Applicant's IDS (hereinafter Kitamura) in view of Nakagawa et al., U.S. Patent Number 5,241,679 (hereinafter Nakagawa). Referring to claim 11, Kitamura has not taught the digital signal processor wherein said storage includes a plurality of registers, said registers automatically transfer existing data from a first register to a second register when new data is being written into said first register. Nakagawa has taught a storage including a plurality of registers (Nakagawa figure 1), where the registers automatically transfer existing data from a first register to a second register when new data is written into the first register (Nakagawa column 4, line 53 to column 5, line 16 and figure 2). Replacing the storage of Kitamura with the multi-register storage of Nakagawa would have allowed for the contents of all the registers to be saved, in case of an interrupt or context switch, simultaneously to the dedicated stack memories in order to perform both saving and restoration at a high speed (Nakagawa column 2, lines 17-23 and 42-49). Therefore, it would have been obvious to a person

of ordinary skill in the art at the time the invention was made to employ the multi-register

storage system of Nakagawa instead of the generic storage means in the system of Kitamura in

order to increase the speed at which context preserving and restoration occurs.

Referring to claim 12, Nakagawa has taught the digital signal processor wherein said

input processor causes the automatic transfer of data (Nakagawa column 4, line 53 to column 5,

line 16 where the processor causing the data to be stored is necessarily an input processor).

Referring to claim 13, Nakagawa has taught the digital signal processor wherein the

mathematical processor causes said data to be transferred from one register to another

(Nakagawa column 4, line 53 to column 5, line 16).

Claim 18 does not recite limitations above the claimed invention set forth in claim 11 and

is therefore rejected for the same reasons set forth in the rejection of claim 11 above.

Claim 19 does not recite limitations above the claimed invention set forth in claim 12 and

is therefore rejected for the same reasons set forth in the rejection of claim 12 above.

Claim 20 does not recite limitations above the claimed invention set forth in claim 13 and

is therefore rejected for the same reasons set forth in the rejection of claim 13 above.

Referring to claim 21, Nakagawa has taught storing a bit which indicates which processor

may controls aid automatic transfer of data from one register to another (Nakagawa column 2,

lines 29-33).

(11)   Response to Argument

Response to Argument-Claim Rejections - 35 USC § 112

➢ On pages 15-16 of the Appeal Brief, Applicant argues in essence:

"Claim 15 was rejected on the grounds that the word "multi-cycled" is indefinite. With respect to the objection to the term "multi-cycled" mathematical processor, a multi-cycle element is explained on page 24, line 15 through page 25, line 16 (and as explained in the material set forth in the summary herein at page 14, last paragraph through the end.

As explained on page 14 infra, the use of multi-cycled elements allows interchangeability without affecting the instruction decode. A busy signal can be used to hold off new data from being sourced to the ineffected unit. Internal delays may be used to match latency such that multi-cycle operation occurs. This allows the various processors in the overall system to be exchanged and changed out regardless of whether they may involve operations spread over two or more clock cycles. For example, input data valid and input destination signals may be delayed that needed number of cycles to make different processors working on different cycles coherent.

Different multi-cycled mathematical processors may be added to the overall process regardless of whether they require more or less time than the processor which they replace. Thus, in cases where a slower math processor is replacing a faster math processor, a multi-cycled architecture may be used to compensate for the additional delay time. The MPC 18 is recompiled when a new processor that is slower or faster is added to adjust to the slower or faster timer of the new processor."

Applicant has claimed a "multi-cycled mathematical processor", not a "multi-cycled

master processor". However, Applicant is appearing to argue that the master processor is multi-

cycled... not the mathematical processor.   On page 25, lines 9-24 of Applicant's specification,

Applicant describes a multi-cycled architecture which is controlled by the master programmable

controller. The master programmable controller adjusts to the speed of the processor, in order to

support a processor no matter what its speed. This appears to be what Applicant is arguing.

It is clear from Applicant's own admissions above that a certain processor has a certain

speed, where certain processors are faster than other certain processors. For one of ordinary skill

in the art, "multi-cycled mathematical processor" is interpreted at least two ways: 1) the

processor requires multiple cycles to complete an operation and 2) that it is operated at various

cycle speeds. The way Applicant is arguing to interpret "Multi-cycled mathematical processor"

is much different than the way one of ordinary skill in the art would interpret "Multi-cycled

mathematical processor". It is not clear from reading the claims as to exactly what a Multi-

cycled mathematical processor is. Furthermore the specification does not specifically clarify

what a Multi-cycled mathematical processor is. There is support for both interpretations in the

specification. On page 24, lines 20-23, Applicant discloses a multi-cycle operation on a

processor which may take more than one cycle to complete, which supports the first meaning of

this phraseology. On page 23 line 19, Applicant discloses a mutli-cycle mathematical processor

that is operated at various speeds, which supports the second meaning. After reading claim 15 in

light of the specification, it is still unclear as to what the metes and bounds are of the claim.

Therefore claim 15 is indefinite.

Response to Argument-Claim Rejections - 35 USC § 102

> On pages 16-17 Applicant argues with respect to claim 1 in essence:

"However, as indicated in column 11 of Kitamura, paragraph 39,

beginning at line 47, the data processing unit 5 splices the video data DA and DB

in response to a splicing instruction from CPU 7. There is no indication that this

device can be considered to be a mathematical processor. Thus, at least one

element is missing in Kitamura and, therefore the Sections 102 rejection should

be reversed.

With respect to the argument that, in essence, "mathematical processor"

simply means any processor, it is clear this cannot be so since mathematical

processor is a well known term of art. Clearly mathematical processors are

processors devoted to doing mathematical operations such as add and subtract.

See, e.g., page 5, lines 17-24. This understanding is further supported by the

attached academic paper.

Therefore, the rejection of claim 1, should be reversed."

However, "Mathematics" as defined by <u>Merriam-Webster's Collegiate Dictionary, Tenth</u>

Edition (see attached) is:

" the science of numbers and their operations, interrelations, combinations,
generalizations, and abstractions and of space configurations and their structure,
measurement, transformations, and generalizations. "

Kitamura has taught that data processing unit 5 splices the video data DA and DB in

response to a splicing instruction. DA and DB are encoded video data, which are

combinations of bits, or numbers. (Kitamura, Column 11, lines 20-25) Since the data

processing unit 5, operates on, or splices numbers representing the coded video data DA

and DB, the data processing unit, as taught by Kitamura, is a mathematical processor.

Furthermore, more specifically, Kitamura has taught in column 26 that the blanking

generator 20 (which is included as a part of the mathematical processor, element 5, See

Figure 6) "produces blanking data D_{BLK} by setting a <u>differential value</u> between a

macroblock and a reference macroblock..." (column 26 lines 45-50). A differential as

defined by <u>Microsoft Press Computer Dictionary, Second Edition</u> (see attached) is:

> *"In electronics, a reference to a type of circuit that makes use of the difference*
>
> *between two signals rather than the difference between one signal and some*
>
> *reference voltage."*

Accordingly, in order to set a differential value or number, the difference of two numbers

must be calculated. "Difference" as defined by <u>Microsoft Press Computer Dictionary,</u>

<u>Second Edition</u> (see attached) is:

> *"The amount by which two values differ. In arithmetic, the difference is the result*
>
> *of subtracting one number from another. In electronics, differences in physical*
>
> *elements, such as waveforms or voltages, are used in the operation of circuits,*
>
> *amplifiers, multiplexers, communications equipment, and so on...."*

Therefore, in order to calculate the difference between two numbers, a subtraction of the

two numbers must be performed. Subtraction is clearly a mathematical operation, as

admitted by Applicant in the argument above. The processor of Kitamura, element 5, is a

mathematical processor because when it sets the differential value between a macroblock

and a reference macroblock, it is performing a mathematical operation.

> On page 17 Applicant argues with respect to claim 16 in essence:

"Similarly, claim 16 calls for using a third processor for mathematical

operations. No such thing is shown in Kitamura."

However, as proven above, Kitamura has in fact taught a third processor for

mathematical operations. (Figure 6, element 5) Therefore, Kitamura has in fact taught

each and every limitation in 16.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Tonia Meonske

TM 2/10/03

February 10, 2003

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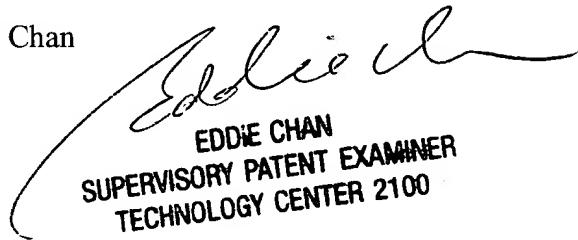
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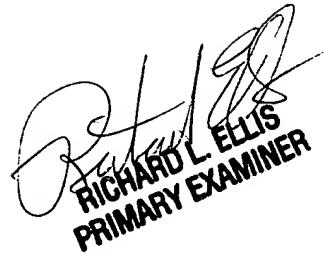
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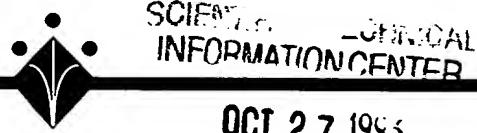
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dibit Pronounced "dye-bit." A set of two bits representing one of four possible combinations: 00, 01, 10, and 11. In communications, a dibit is a kind of transmission unit made possible by the modulation technique known as differential phase-shift keying, which encodes data by using four different states (phase shifts) in the transmission line to represent each of the four dibit combinations. *See also* phase-shift keying.

dichotomizing search *See* binary search.

DIF *See* data interchange format.

difference The amount by which two values differ. In arithmetic, the difference is the result of subtracting one number from another. In electronics, differences in physical elements, such as waveforms or voltages, are used in the operation of circuits, amplifiers, multiplexers, communications equipment, and so on.

In database management, an operator in the relational algebra used in sorting records (tuples). For example, given two relations (tables), A and B, that are union-compatible (contain the same number of fields, with corresponding fields containing the same types of values),

DIFFERENCE A, B

builds a third relation containing all those records that appear in A but not in B. *Compare* intersect, union.

Difference Engine An early computerlike mechanical device designed by British mathematician and scientist Charles Babbage in the early 1820s. Although never completed by Babbage, the Difference Engine was intended to be a machine with a 20-decimal capacity capable of solving mathematical problems. The concept of the Difference Engine was enhanced by Babbage in the 1830s in the design of his more famous Analytical Engine, a mechanical precursor of the electronic computer. Babbage, incidentally, was also the inventor of the speedometer and the cowcatcher. *See also* Analytical Engine.

differential In electronics, a reference to a type of circuit that makes use of the difference between two signals rather than the difference between one signal and some reference voltage.

differential phase-shift keying *See* phase-shift keying.

differentiator A circuit whose output is the differential (first derivative) of the input signal. The differential measures how fast a value is changing, so the output of a differentiator is proportional to the instantaneous rate of change of the input signal, as shown in the illustration. *Compare* integrator.
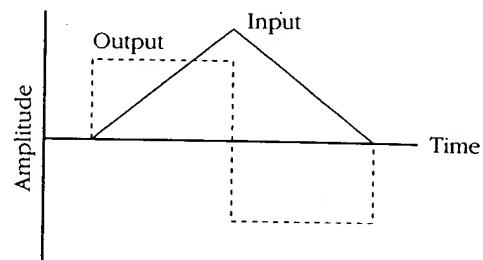

Differentiator.
An example of the action of a differentiator circuit.

digit One of the characters used to indicate a whole number (unit) in a numbering system. In any numbering system, the number of possible digits is equal to the base, or radix, used. For example, the decimal (base-10) system has 10 digits, 0 through 9; the binary (base-2) system has two digits, 0 and 1; and the hexadecimal (base-16) system has 16 digits, 0 through 9 and A through F.

digital Related to digits or the way they are represented. In computing, *digital* is virtually synonymous with *binary* because the computers familiar to most people process information coded as combinations of binary digits (bits). One bit can represent at most two values; 2 bits, four values; 8 bits, two hundred fifty-six values; and so on. Values that fall between two numbers are represented as either the lower or the higher of the two. Because digital representation represents a value as a coded number, the range of values represented can be very wide, although the number of possible values is limited by the num-
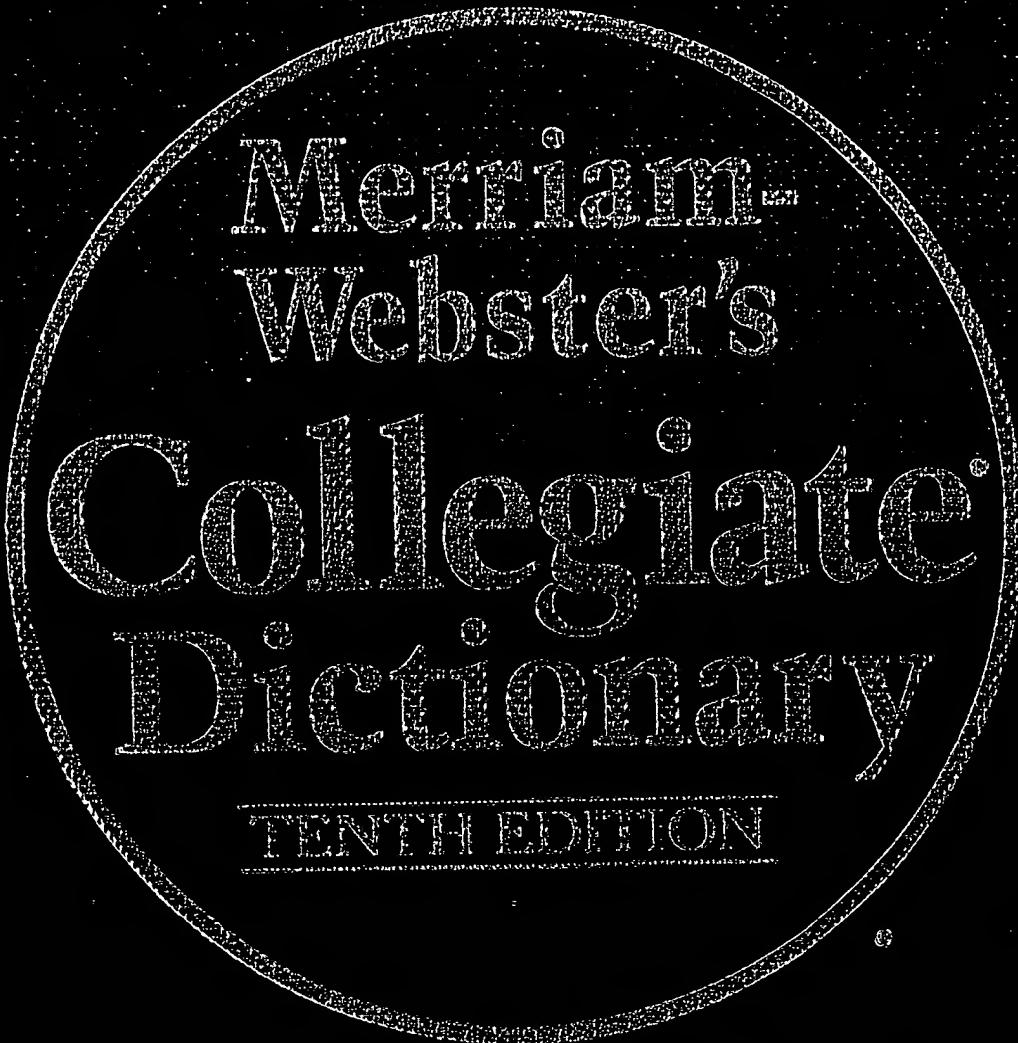
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nastiche, fr. G̱
: an aromatic ṁ
ishes 2 : any
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⸳⸳⸳, fr. MF *meiche*] (1549), 1 : a chemically prepared
⸳⸳⸳ used in firing firearms or powder 2 : a short
⸳⸳⸳ material (as wood) tipped with a combusti-
⸳⸳⸳ into flame when slightly heated through fric-
⸳⸳⸳ against a rough surface)
⸳⸳⸳ -bȯrd, -ᵻbȯrd\ n (ca. 1858) : a board with a groove
⸳⸳⸳ a tongue along the other so as to fit snugly with
⸳⸳⸳ cut boards
⸳⸳⸳ n (1944) : a small folder containing rows of paper

⸳⸳⸳ (1786) : a box for matches
⸳⸳⸳ (ca. 1530) : having no equal : PEERLESS — **match-**

⸳⸳⸳ (1637) 1 : a slow-burning match lowered over a
⸳⸳⸳ of a musket to ignite the charge 2 : a musket
⸳⸳⸳ **matchlock**
⸳⸳⸳-kȯr\ n (ca. 1639) : one that arranges a match; esp
⸳⸳⸳ two unmarried individuals together in an at-
⸳⸳⸳ a marriage — **match·mak·ing** \-kiŋ\ n
⸳⸳⸳ : golf competition in which the winner is the per-
⸳⸳⸳ the greater number of holes — compare STROKE

⸳⸳⸳ : a situation (as in tennis) in which one player or
⸳⸳⸳ by winning the next point; *also* : the point itself
⸳⸳⸳-stik\ n (1791) 1 : a slender piece esp. of wood
⸳⸳⸳ is made 2 : something resembling a matchstick

⸳⸳⸳(1964) : ¹MATCH
⸳⸳⸳\ n (1838) : small pieces of wood : SPLINTERS
⸳⸳⸳ed; mat·ing [ME, fr. MF *mater*, fr. OF *mat*, n.,
⸳⸳⸳mār (in *shāh māt*)] (14c) : CHECKMATE 2
⸳⸳⸳CKMATE 1
⸳⸳⸳fr. MLG *māt*; akin to OE *gemetta* guest at one's ta-
⸳⸳⸳more at MEAT] (14c) 1 a (1) : ASSOCIATE, COMPAN-
⸳⸳⸳an assistant to a more skilled worker : HELPER
⸳⸳⸳END, BUDDY — often used as a familiar form of ad-
⸳⸳⸳MATCH, PEER 2 : a deck officer on a merchant ship
⸳⸳⸳captain 3 : one of a pair: as a : either member of a
⸳⸳⸳married couple b : either member of a breeding pair
⸳⸳⸳er of two matched objects
⸳⸳⸳ing vt (1509) 1 archaic : EQUAL, MATCH 2 : to
⸳⸳⸳COUPLE 3 a : to join together as mates b : to
⸳⸳⸳ vi 1 : to become mated ⟨gears that ~ well⟩ 2

⸳⸳⸳\n [F & AmerSp; F maté, fr. AmerSp mate
⸳⸳⸳king it, fr. Quechua *mati* vessel] (1758) 1 : a tea-
⸳⸳⸳ esp. in So. America 2 : a So. American shrub or
⸳⸳⸳ of the holly family whose leaves and shoots
⸳⸳⸳maté; *also* : these leaves and shoots
⸳⸳⸳-tə-\ n [F, fr. MF, fr. MD *mattenoot*, lit., bed-
⸳⸳⸳AILOR
⸳⸳⸳, mat-ᵻlȯt\ n [F, lit., sailor's wife, fr. *matelot*] (ca.
⸳⸳⸳ of fish in a seasoned wine sauce
⸳⸳⸳[L — more at MOTHER] (ca. 1859) *chiefly Brit*

⸳⸳⸳tǝr-ᵻə-'mi-lē-əs, -ᵻmä-\ n [L, fr. *mater + familias*,
⸳⸳⸳household — more at FAMILY] (1756) : a woman
⸳⸳⸳household
⸳⸳⸳ə\ adj [ME *materiel*, fr. MF & LL; MF, fr. LL
⸳⸳⸳ia matter — more at MATTER] (14c) 1 a (1) : re-
⸳⸳⸳or consisting of matter; *esp* : PHYSICAL ⟨the ~
⸳⸳⸳⟨~ needs⟩ b (1) : of or relating to matter rather
⸳⸳⸳ (2) : of or relating to the subject matter of rea-
⸳⸳⸳CAL ⟨~ knowledge⟩ 2 : having real importance
⸳⸳⸳ ⟨facts ~ to the investigation⟩ 3 a : being of a
⸳⸳⸳nature b : relating to or concerned with physical
⸳⸳⸳or intellectual things ⟨~ progress⟩ — **ma·te·ri-**
⸳⸳⸳**ma·te·ri·al·ness** n
⸳⸳⸳YSICAL, CORPOREAL, PHENOMENAL, SENSIBLE, OB-
⸳⸳⸳ belonging to actuality. MATERIAL implies forma-
⸳⸳⸳e matter, used in contrast with *spiritual* or *ideal* it
⸳⸳⸳mundane, crass, or grasping ⟨*material* values⟩.
⸳⸳⸳al what is perceived directly by the senses and may
⸳⸳⸳ spiritual, or imaginary ⟨the *physical* benefits of
⸳⸳⸳REAL implies having the tangible qualities of a body
⸳⸳⸳or resistance to force ⟨artists have portrayed an-
⸳⸳⸳tions⟩. PHENOMENAL applies to what is known or
⸳⸳⸳the senses rather than by intuition or rational de-
⸳⸳⸳concerned with the *phenomenal* world). SENSIBLE
⸳⸳⸳ity of readily or forcibly impressing the senses ⟨the
⸳⸳⸳not *sensible* to us⟩. OBJECTIVE may stress a matriard
⸳⸳⸳ence apart from a subject perceiving it ⟨no *objec-*
⸳⸳⸳age⟩. *syn* see in addition RELEVANT
⸳⸳⸳a (1) : the elements, constituents, or substances of
⸳⸳⸳composed or can be made (2) : matter that has
⸳⸳⸳individuality and by which it may be characterized
⸳⸳⸳⟨~⟩ b (1) : something (as data) that may be
⸳⸳⸳finished from ⟨~ for a biography⟩ (2) : some-
⸳⸳⸳de the object of study ⟨~ for the next semester⟩
⸳⸳⸳repertoire ⟨a comedian's ~⟩ c : MATTER 3b d
⸳⸳⸳ potentially suited to some pursuit ⟨varsity ~⟩
⸳⸳⸳a : apparatus necessary for doing or making some-
⸳⸳⸳b : MATÉRIEL
⸳⸳⸳*var of* MATERIALIZE
⸳⸳⸳tür-ē-ə-ᵻli-zəm\ n (1748) 1 a : a theory that physi-
⸳⸳⸳y or fundamental reality and that all being and pro-
⸳⸳⸳na can be explained as manifestations or results of
⸳⸳⸳ that the only or the highest values or objectives
⸳⸳⸳ing and in the furtherance of material progress c
⸳⸳⸳economic or social change is materially caused —
⸳⸳⸳AL MATERIALISM 2 : a preoccupation with or stress
⸳⸳⸳er than intellectual or spiritual things — **ma·te·ri-**
⸳⸳⸳**-k(ə-)ri·al·is·tic** \-ᵻtir-ē-ə-'lis-tik\ adj — **ma·te-**
⸳⸳⸳k(ə-)lē\ adv

ma·te·ri·al·i·ty \mə-ᵻtir-ē-'a-lə-tē\ n, pl **-ties** (1570) 1 : the quality or
state of being material 2 : something that is material
ma·te·ri·al·i·za·tion \mə-ᵻtir-ē-ə-lə-'zā-shən\ n (1843) 1 : the action of
materializing or becoming materialized 2 : something that has been
materialized; esp : APPARITION
ma·te·ri·al·ize \mə-'tir-ē-ə-ᵻlīz\ vb **-ized; -iz·ing** vt 1 a : to make
material : OBJECTIFY b : to cause to appear in bodily form ⟨~ the
spirits of the dead⟩ 2 : to cause to be materialistic ~ vi 1 : to assume
bodily form 2 a : to appear esp. suddenly b : to come into existence
— **ma·te·ri·al·iz·er** n
materials science n (1961) : the scientific study of the properties and
applications of materials of construction or manufacture (as ceramics,
metals, polymers, and composites) — **materials scientist** n
ma·te·ria med·i·ca \mə-ᵻtir-ē-ə-'me-di-kə\ n [NL, lit., medical matter]
(1699) 1 : substances used in the composition of medical remedies
: DRUGS, MEDICINE 2 a : a branch of medical science that deals with
the sources, nature, properties, and preparation of drugs b : a treatise
on materia medica
ma·té·ri·el or **ma·te·ri·el** \mə-ᵻtir-ē-'el\ n [F *matériel*, fr. *matériel*, adj.]
(1814) : equipment, apparatus, and supplies used by an organization or
institution
ma·ter·nal \mə-'tər-nᵊl\ adj [ME, fr. MF *maternel*, fr. L *maternus*, fr.
mater mother — more at MOTHER] (15c) 1 : of, relating to, belonging
to, or characteristic of a mother : MOTHERLY 2 a : related through a
mother ⟨his ~ aunt⟩ b : inherited or derived from the female parent
⟨~ genes⟩ — **ma·ter·nal·ly** \-nᵊl-ē\ adv
¹**ma·ter·ni·ty** \mə-'tər-nə-tē\ n, pl **-ties** (1611) 1 a : the quality or state
of being a mother : MOTHERHOOD b : the qualities of a mother
: MOTHERLINESS 2 : a hospital facility designed for the care of women
before and during childbirth and for the care of newborn babies
²**maternity** adj (1893) 1 : designed for wear during pregnancy ⟨a ~
dress⟩ 2 : effective for the period close to and including childbirth
⟨~ leave⟩
mat·ey \'mā-tē\ adj (1915) *chiefly Brit* : COMPANIONABLE — **mat·ey-**
ness \-nəs\ n, *chiefly Brit*
math \'math\ n (ca. 1878) : MATHEMATICS
math·e·mat·i·cal \ᵻmath-'ma-ti-kəl, ᵻma-thə-\ *also* **math·e·mat·ic** \-tik\
adj [ME *mathematicalle*, fr. L *mathematicus*, fr. Gk *mathēmatikos*, fr.
mathēmat-, mathēma learning, mathematics, fr. *manthanein* to learn;
prob. akin to Goth *mundon* to pay attention] (15c) 1 : of, relating to,
or according with mathematics 2 a : rigorously exact : PRECISE b
: CERTAIN 3 : possible but highly improbable ⟨only a ~ chance⟩ —
math·e·mat·i·cal·ly \-ti-k(ə-)lē\ adv
mathematical expectation n (1838) : EXPECTED VALUE
mathematical induction n (1838) : INDUCTION 2b
mathematical logic n (1858) : SYMBOLIC LOGIC
math·e·ma·ti·cian \ᵻmath-mə-'ti-shən, ᵻma-thə-\ n (15c) : a specialist or
expert in mathematics
math·e·mat·ics \ᵻmath-'ma-tiks, ᵻma-thə-\ n pl but usu sing in constr
(1581) 1 : the science of numbers and their operations, interrelations,
combinations, generalizations, and abstractions and of space configu-
rations and their structure, measurement, transformations, and general-
izations 2 : a branch of, operation in, or use of mathematics ⟨the ~
of physical chemistry⟩
math·e·ma·ti·za·tion \ᵻmath-mə-tə-'zā-shən, ᵻma-thə-\ n (1928) : reduc-
tion to mathematical form — **math·e·ma·tize** \'math-mə-ᵻtiz, 'ma-
thə-\ vb
maths \'maths\ n pl (1911) *chiefly Brit* : MATHEMATICS
mat·in \'ma-tᵊn\ adj [ME, fr. OF] (14c) : of or relating to matins or to
early morning
mat·in·al \'ma-tᵊn-əl\ adj (1803) 1 : of or relating to matins 2 : EARLY
mat·i·nee or **mat·i·née** \ᵻma-tᵊn-'ā\ n [F *matinée*, lit., morning, fr. OF,
fr. *matin* morning, fr. L *matutinum*, fr. neut. of *matutinus* of the morn-
ing, fr. *Matuta*, goddess of morning; akin to L *maturus* ripe — more at
MATURE] (1858) : a musical or dramatic performance or social or pub-
lic event held in the daytime and esp. the afternoon
matinee idol n (1902) : a handsome male performer
mat·ins \'ma-tᵊnz\ n pl but sing or pl in constr, often cap [ME *matines*, fr.
OF, fr. LL *matutinae*, fr. L, fem. pl. of *matutinus*] (14c) 1 : the night
office forming with lauds the first of the canonical hours 2 : MORN-
ING PRAYER
matr- or **matri-** or **matro-** comb form [L *matr-, matri-*, fr. *matr-, mater*]
: mother ⟨*matri*arch⟩ ⟨*matro*nymic⟩
ma·tri·arch \'mā-trē-ᵻärk\ n (1606) : a female who rules or dominates a
family, group, or state; *specif* : a mother who is head and ruler of her
family and descendants — **ma·tri·ar·chal** \ᵻmā-trē-'är-kəl\ adj
ma·tri·ar·chate \'mā-trē-ᵻär-kət, -ᵻkāt\ n (1885) : MATRIARCHY 1
ma·tri·ar·chy \'mā-trē-ᵻär-kē\ n, pl **-chies** (1885) 1 : a family, group, or
state governed by a matriarch 2 : a system of social organization in
which descent and inheritance are traced through the female line
ma·tri·cide \'ma-trə-ᵻsīd, 'mā-\ n (1594) 1 [L *matricidium*, fr. *matr-* +
-cidium -cide] : murder of a mother by her son or daughter 2 [L *matri-
cida*, fr. *matr-* + *-cida* -cide] : one that murders his or her mother —
ma·tri·cid·al \ᵻma-trə-'sī-dᵊl, ᵻmā-\ adj
ma·tric·u·late \mə-'tri-kyə-ᵻlāt\ vb **-lat·ed; -lat·ing** [ML *matriculatus*,
pp. of *matriculare*, fr. LL *matricula* public roll, dim. of *matric-, matrix*
list, fr. L, breeding female] vt (1577) : to enroll as a member of a body
and esp. of a college or university ~ vi : to become matriculated —
ma·tric·u·lant \-lənt\ n — **ma·tric·u·la·tion** \-ᵻtri-kyə-'lā-shən\ n
ma·tri·lin·eal \ᵻma-trə-'li-nē-əl, ᵻmā-\ adj (1904) : relating to, based on,
or tracing descent through the maternal line ⟨~ society⟩ — **ma·tri-**
lin·eal·ly \-nē-ə-lē\ adv
mat·ri·mo·nial \ᵻma-trə-'mō-nē-əl, -nyəl\ adj (15c) : of or relating to
marriage, the married state, or married persons — **mat·ri·mo·nial·ly**
adv

\ə\ abut \ᵊ\ kitten, F table \ər\ further \a\ ash \ā\ ace \ä\ mop, mar
\au̇\ out \ch\ chin \e\ bet \ē\ easy \g\ go \i\ hit \ī\ ice \j\ job
\ŋ\ sing \ō\ go \ȯ\ law \ȯi\ boy \th\ thin \t͟h\ the \ü\ loot \u̇\ foot
\y\ yet \zh\ vision \à, ḵ, ᵊ, œ, œ̄, ᵫ, ǣ, ꞑ\ see Guide to Pronunciation